

*Design Vision Network*

# Architectures and Systems

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# Motivations

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- Help the UK microelectronic industry
  - challenge since there are many SMEs but no really big players (>1000 employees) in the UK
  - supply of well educated EE/CS graduates and PhDs is probably the most direct contribution
  - industry needs to encourage this activity by encouraging research since this feeds back into the teaching
  - startups
- Improve research and education in microelectronic architectures and systems
  - we need to coordinate expertise at multiple universities and companies to make this happen

# Improving Communication

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- Academic Forums
  - tutorial + platform for PhD students
- Hot topic meetings
  - invited industry and academic experts
- Coordination and Policy
  - e.g. UKDF

# Academic Forums

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- UK Async Forum
  - has been very successful in promoting async. circuit design in the UK
  - but many “async” groups now have a broader remit
  - transform the event into the:  
**UK Digital Circuits and Systems Forum?**
  - needs to be complementary to PREP
- UK ACM Special Interest Group in Design Automation
  - needs reviving or amalgamating?

# Hot topic meetings

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- Get leading lights in industry and academia together to talk about a focused hot topic
- e.g. like the IEE Cambridge Branch annual seminar
  - Last year: Processor Cores – Putting Silicon IP To Work
  - This Dec: Mobile TV Technologies – Evolution or Revolution?
- Should we do more in this space as part of the design vision?

# Coordination and Policy

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- UKDF and various meetings at IEE seem to fill this role
- Do we need anything else?

# Timeliness

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- Exciting time for computer architecture research:
  - Shift from uni-processor to chip multiprocessors, “many-core” and beyond...
  - Shift to communication-centric design
    - e.g. use of on-chip networks
    - Need to reevaluate communication/computation trade-offs
  - Performance increasingly limited by complexity, communication and power
- Further out things get even more interesting:
  - Reliability set to become a major design challenge
    - 100B transistors on-a-chip, 20% unusable after manufacture, 10% fail over time + intermittent failures [Borkar03]
  - Multi-layer packaging structures, CMOS + nanotechnology layer, ...